Application No.: 09/606,734

REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Claims 1 and 4 stand rejected under 35 USC 112. Such claims point out that the method includes "passing messages through the message network with such passing messages by-passing the data transfer section". Support is shown, *inter alia*, in connection with FIG. 2.

It is first noted that ***user data*** passes between the host computer /server and the bank of disk drives through the cache memory 220; however, the ***messages*** which control the user data pass ***between the directors through*** the ***message network 260 without*** going through the cache memory 220 and therefore these ***messages*** thereby ***by-pass*** the cache memory 220. FIG. 2 shows that ***messages***, pass from any director (more particularly from the message engine/CPU controller 314 thereof) to the ***message network 260*** and then to one or more other directors ***without passing through*** the global cache memory 220; that is, the ***messages*** pass through the message network and ***by-pass*** the global cache memory. It is respectfully submitted that it is clear from the text and FIG. 2 that the ***messages*** pass through the ***message network*** and DO NOT PASS THROUGH BUT RATHER PASS BY OR BY-PASS the global cache memory. It is noted that ***user data*** passing between the host computer and the bank of disk drives passes through the global cache memory the ***messages*** used to control the user data DO NOT PASS THROUGH THE CACHE MEMORY BY RATHER BY-PASS THE CACHE MEMORY 220 and pass through the message network 260.

Reference is made to page 7, lines 15 through page 8 line 15 of the patent application:

> Referring now to FIG. 2, a data storage system 100 is shown for transferring data between a host computer/server 120 and a bank of disk drives 140 through a system interface 160. The system interface 160 includes: a plurality of, here 32 front-end directors 180_1-180_{32} coupled to the host

computer/server 120 via ports-123_{32}; a plurality of back-end directors 200_1-200_{32} coupled to the bank of disk drives 140 via ports 123_{33}-123_{64}; a data transfer section 240, having a global cache memory 220, coupled to the plurality of front-end directors 180_1-180_{16} and the back-end directors 200_1-200_{16}; and a messaging network 260, operative independently of the data transfer section 240, coupled to the plurality of front-end directors 180_1-180_{32} and the plurality of back-end directors 200_1-200_{32}, as shown. The front-end and back-end directors 180_1-180_{32}, 200_1-200_{32} are functionally similar and include a microprocessor (μP) 299 (i.e., a central processing unit (CPU) and RAM), a message engine/ CPU controller 314 and a data pipe 316 to be described in detail in connection with FIGS. 5, 6 and 7. ***Suffice it to say here, however, that the front-end and back-end directors 180_1-180_{32}, 200_1-200_{32} control data transfer between the host computer/server 120 and the bank of disk drives 140 in response to messages passing between the directors 180_1-180_{32}, 200_1-200_{32} through the messaging network 260.*** The messages facilitate the data transfer between host computer/server 120 and the bank of disk drives 140 with such data passing through the global cache memory 220 via the data transfer section 240. ***More particularly, in the case of the front-end directors 180_1-180_{32}, the data passes between the host computer to the global cache memory 220 through the data pipe 316 in the front-end directors 180_1-180_{32} and the messages pass through the message engine/CPU controller 314 in such front-end directors 180_1-180_{32}. In the case of the back-end directors 200_1-200_{32} the data passes between the back-end directors 200_1-200_{32} and the bank of disk drives 140 and the global cache memory 220 through the data pipe 316 in the back-end directors 200_1-200_{32} and again the messages pass through the message engine/CPU controller 314 in such back-end director 200_1-200_{32}.***

With such an arrangement, the cache memory 220 in the data transfer section 240 is not burdened with the task of transferring the director messaging. Rather the messaging network 260 operates independent of the data transfer section 240 thereby increasing the operating bandwidth of the system interface 160. (Emphasis added)

In view of the foregoing it is respectfully submitted that the claims 1 and 4 are in accordance with 35 USC paragraph 112. The Examiner is respectfully requested to point to any portion of the patent application that indicates that the ***messages***, as distinguished from the data, pass through the cache memory.

Claims 7, 8, 15 and 16 have been amended to correct a typographical error and now point out that the bank of is a bank of disk drives.

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Claim 1 and 4 stand rejected under 35 USC 102 (e) as being anticipated by Chung et al. (USP 6,470,389). Applicant fails to find in Chung et al:

> a plurality of second directors coupled to the bank of disk drives; a data transfer section having a cache memory coupled to the plurality of first directors and second directors; and a messaging network coupled to the plurality of first directors and the plurality of second directors, such method comprising:
>
> passing messages through the message network with such passing messages by-passing the cache memory; (emphasis added)

Claims 7 and 15 stand rejected under 365 USC 103 as being unpatentable over Chung et al (USP 6,470,389) in view of Etheridge et al. (USP 6,466,572). As noted above:, applicant fails to find in Chung et al:

> a plurality of second directors coupled to the bank of disk drives; a data transfer section having a cache memory coupled to the plurality of first directors and second directors; and a messaging network coupled to the plurality of first directors and the plurality of second directors, such method comprising:
>
> passing messages through the message network with such passing messages by-passing the cache memory; (emphasis added)

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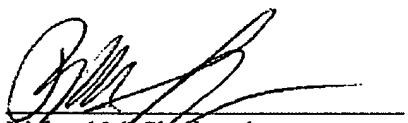
Respectfully submitted,

Nov 7, 2005
Date



Richard M. Sharkansky
Attorney for Applicant(s)
Reg. No.: 25,800
P. O. Box 557
Mashpee, MA 02649
Telephone: (508) 477-4311
Facsimile: (508) 477-7234